zbMATH Open
THE FIRST RESOURCE FOR MATHEMATICS

Leighton, Tom; **Leiserson, Charles E.**
Wafer-scale integration of systolic arrays. (English) Zbl 0558.94020
IEEE Trans. Comput. 34, 448-461 (1985).

VLSI technologists are fast developing wafer-scale integration. Rather than partitioning a silicon wafer into chips as is usually done, the idea behind wafer-scale integration is to assemble an entire system (or network of chips) on a single wafer, thus avoiding the costs and performance loss associated with individual packaging of chips. A major problem with assembling a large system of microprocessors on a single wafer, however, is that some of the processors, or cells, on the wafer are likely to be defective. In the paper, we describe practical procedures for integrating "around" such faults. The procedures are designed to minimize the length of the longest wire in the system, thus minimizing the communication time between cells. Although the underlying network problems are NP-complete, we prove that the procedures are reliable by assuming a probabilistic model of cell failure. We also discuss applications of the work to problems in VLSI layout theory, graph theory, fault-tolerant systems, planar geometry, and the probabilistic analysis of algorithms.

Reviewer: Reviewer (Berlin)

MSC:

94C15 Applications of graph theory to circuits and networks
68N99 Theory of software
68Q80 Cellular automata (computational aspects)

Cited in **13** Documents

Keywords:

fault-tolerant systems; probabilistic analysis; spanning tree; traveling salesman; VLSI

Full Text: DOI

Edited by FIZ Karlsruhe, the European Mathematical Society and the Heidelberg Academy of Sciences and Humanities
© 2021 FIZ Karlsruhe GmbH