Gregoretti, Francesco; **Passerone, Roberto**; **Reyneri, Leonardo Maria**; **Sansoé, Claudio**
A high speed VLSI architecture for handwriting recognition. (English) Zbl 0987.68847
J. VLSI Signal Process. Syst. Signal Image Video Technol. 28, No. 3, 259-278 (2001).

Summary: This article presents PAPRICA-3, a VLSI-oriented architecture for real-time processing of images and its implementation on HACRE, a high-speed, cascadable, 32-processors VLSI slice. The architecture is based on an array of programmable processing elements with the instruction set tailored to image processing, mathematical morphology, and neural networks emulation. Dedicated hardware features allow simultaneous image acquisition, processing, neural network emulation, and a straightforward interface with a hosting PC.

HACRE has been fabricated and successfully tested at a clock frequency of 50 MHz. A board hosting up to four chips and providing a 33 MHz PCI interface has been manufactured and used to build BEATRIX, a system for the recognition of handwritten check amounts, by integrating image processing and neural network algorithms (on the board) with context analysis techniques (on the hosting PC).

MSC:

68U99 Computing methodologies and applications
68T10 Pattern recognition, speech recognition

Keywords:

PAPRICA-3; VLSI-oriented architecture

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