Pagli, Linda; **Pucci, Geppino**
Counting the number of fault patterns in redundant VLSI arrays. (English) Zbl 0796.94022
Inf. Process. Lett. 50, No. 6, 337-342 (1994).

Summary: In VLSI technology, redundancy is a commonly adopted technique to provide reconfiguration capabilities to regular architectures. This paper proves upper and lower bounds on the number of minimal fault patterns (minimal set of faulty processors) which affect a link-redundant linear array in an unrepairable way, for both the cases of bidirectional and unidirectional links.

MSC:

94C12	Fault detection; testing in circuits and networks	Cited in **5** Documents
68M20	Performance evaluation, queueing, and scheduling in the context of computer systems	

Keywords:

distributed systems; fault tolerance; parallel processing; performance evaluation; VLSI circuits; upper and lower bounds; number of minimal fault patterns

Full Text: DOI

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